

# ALINX AN8238 2 Channel High Speed AD Module User Manual

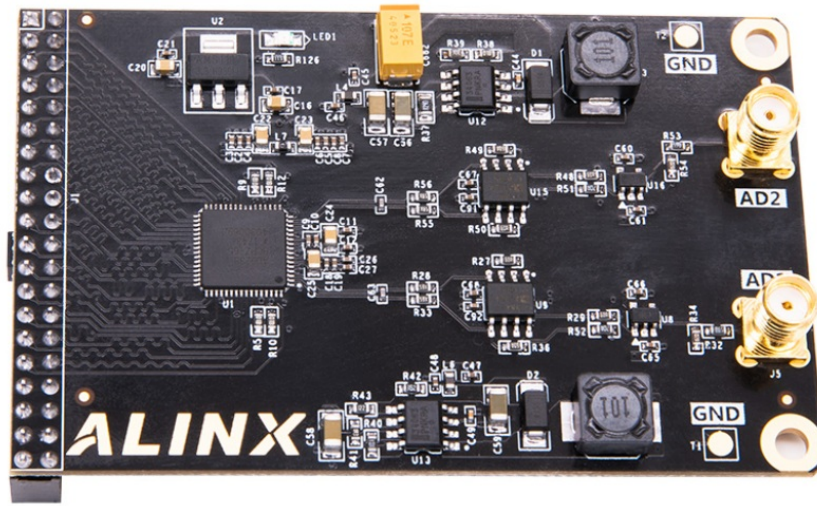
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**ALINX AN8238 2 Channel High Speed AD Module**



## Part 1: 2-Channel High Speed AD Module AN9238

ALINX high-speed AD module AN9238 is a 2-channel 65MSPS, 12-bit analog signal to digital signal module. The AD conversion of the module adopts the AD9238 chip of ADI Company. The AD9238 chip supports 2-channel AD input conversion, so one AD9238 chip supports 2-channel AD input conversion. The analog signal input supports single-ended analog signal input, the input voltage range is  $-5V \sim +5V$ , and the interface is an SMA socket. The module has a standard 0.1 pitch 40-pin female header for connecting to the FPGA development board

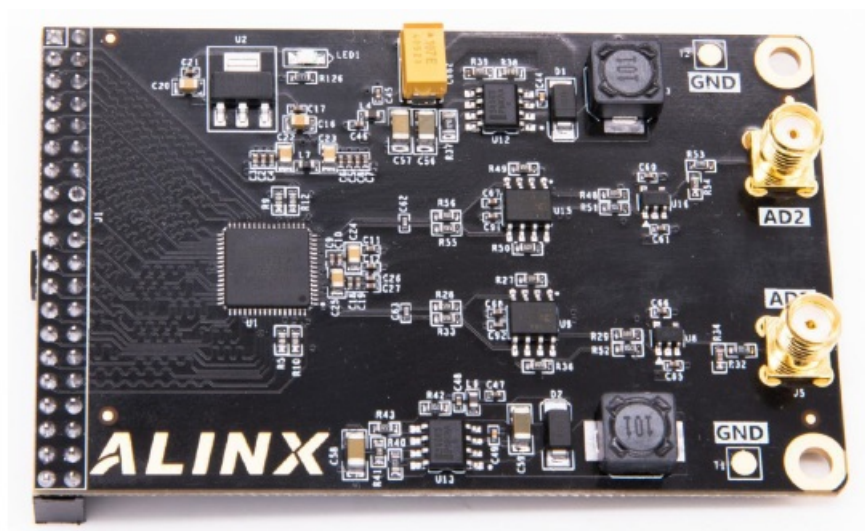


Figure 1-1: AN9238 Module Product Image

### Part 1.1: AN9238 Module Parameter Description

The following are the detailed parameters of the high-speed AD module AN9238:

- AD conversion chip: 1 piece of AD9238
- AD conversion channel: 2 channels;
- AD sampling rate: 65MSPS;
- AD sampling data bits: 12 bits;
- Digital interface level standard: +3.3V CMOS level
- AD analog signal input range:  $-5V \sim +5V$
- Analog signal input interface: SMA interface
- Measurement accuracy: about 10Mv
- Working temperature:  $-40^{\circ} \sim 85^{\circ}$

Part 1.2: AN9238 Module Size Dimension

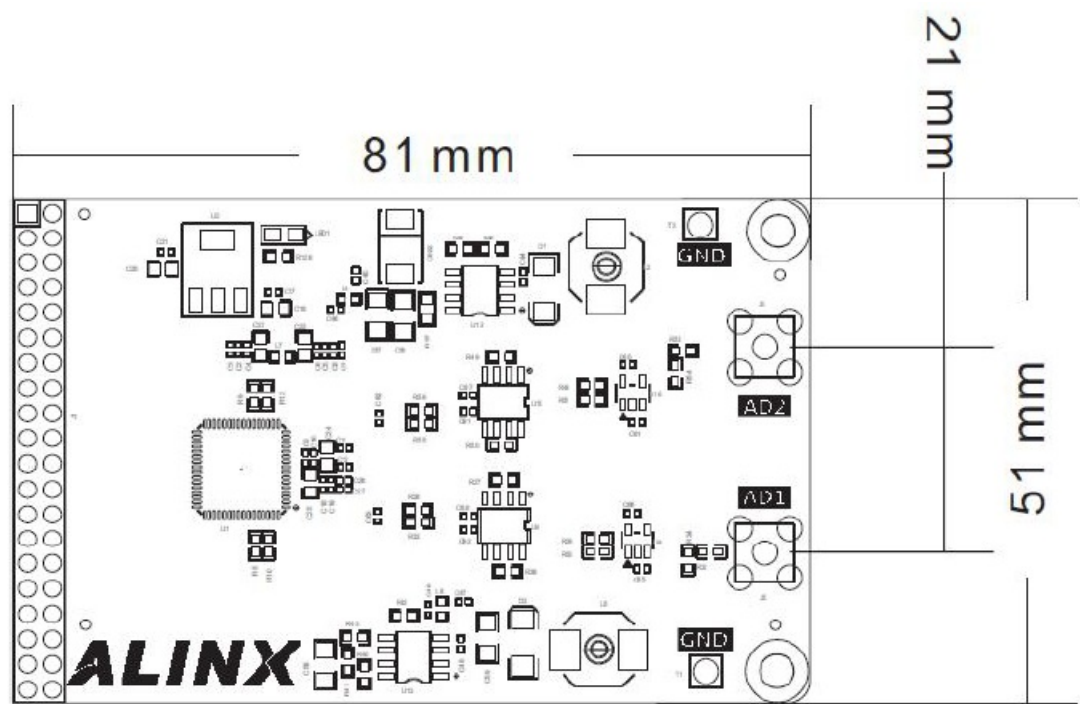


Figure 1-2: AN9238 Module Size Dimension

Part 2: AN9238 Module Function Description

Part 2.1: AN9238 Module Hardware Block Diagram

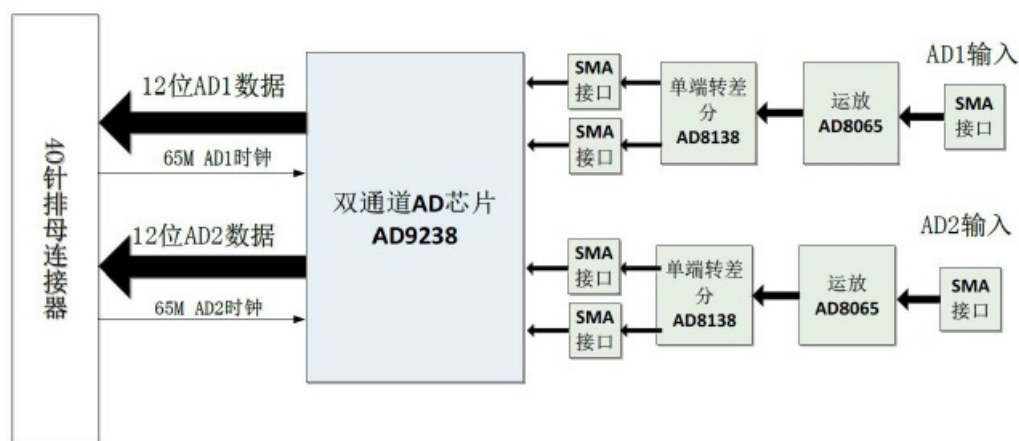


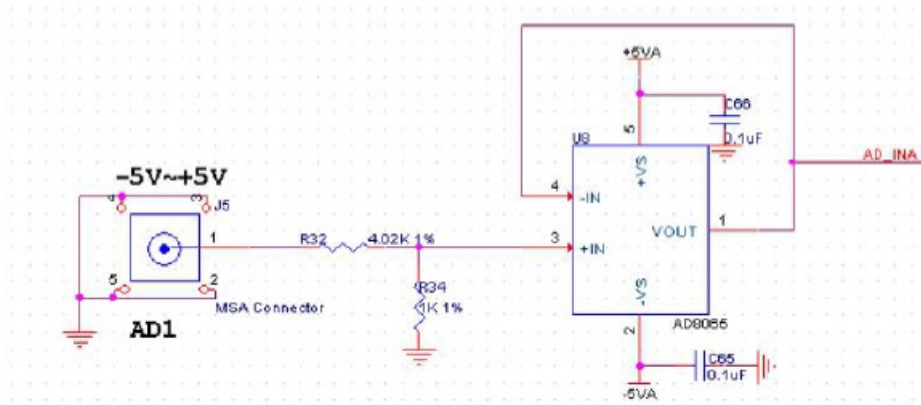
Figure 2-1: AN9238 Module Hardware Block Diagram

For the specific reference design of the AD9238 circuit, please refer to the AD9238 chip manual.

Part 2.1: Single-ended Input and Operational Amplifier Circuit

The single-ended input AD1 and AD2 are input through two SMA headers, J5 or J6, and the voltage of the single-ended input is -5V~+5V. On the FPGA development board, the input voltage of -5V~+5V is reduced to -1V~+1V through the AD8065 chip and voltage divider resistors. If the user wants to input a wider range of voltage, just modify the resistance of the front-end voltage divider resistor.

Conversion Formula:  $V_{OUT} = (1.0/5.02) \cdot V_{IN}$

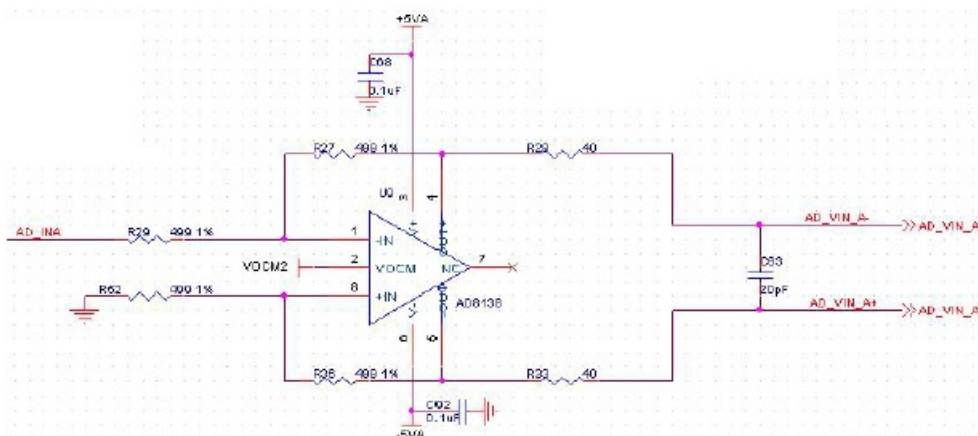


The following table is the voltage comparison table after analog input signal and AD8065 operational amplifier output:

| AD Analog Input Value | AD8065 Operational Amplifier Output |
|-----------------------|-------------------------------------|
| -5 V                  | -1 V                                |
| 0 V                   | 0 V                                 |
| +5 V                  | +1 V                                |

## Part 2.2: Single-ended to Differential and AD Conversion

The input voltage of -1V~+1V is converted into a differential signal ( $V_{IN+} - V_{IN-}$ ) by the AD8138 chip, and the common mode level of the differential signal is determined by the CML pin of AD.



The following table is the voltage comparison table after analog input signal to AD8138 differential output:

| AD Analog Input Value | AD8065 Operational Amplifier Output | AD8138 Differential Output ( $V_{IN+} - V_{IN-}$ ) |
|-----------------------|-------------------------------------|----------------------------------------------------|
| -5 V                  | -1 V                                | -1 V                                               |
| 0 V                   | 0 V                                 | 0 V                                                |
| +5 V                  | +1 V                                | +1 V                                               |

## Part 2.4: AD9238 Conversion

The default AD is configured as offset binary, and the value of AD conversion is shown in the figure below:

**Table 16. Output Data Format**

| Input (V)           | Condition (V)                  | Offset Binary Output Mode |
|---------------------|--------------------------------|---------------------------|
| $V_{IN+} - V_{IN-}$ | $< -V_{REF} - 0.5 \text{ LSB}$ | 0000 0000 0000            |
| $V_{IN+} - V_{IN-}$ | $= -V_{REF}$                   | 0000 0000 0000            |
| $V_{IN+} - V_{IN-}$ | $= 0$                          | 1000 0000 0000            |
| $V_{IN+} - V_{IN-}$ | $= +V_{REF} - 1.0 \text{ LSB}$ | 1111 1111 1111            |
| $V_{IN+} - V_{IN-}$ | $> +V_{REF} - 0.5 \text{ LSB}$ | 1111 1111 1111            |

In the module circuit design, the VREF value of AD9238 is 1V, so the final analog signal input and AD conversion data are as follows

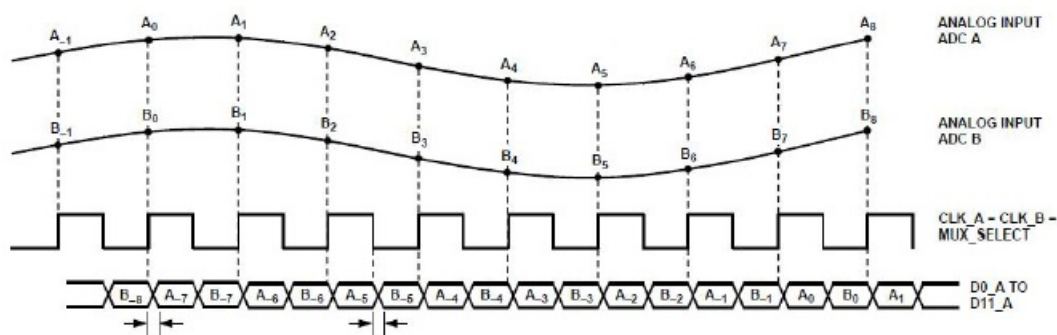
| AD Analog Input Value | AD8065 Operational Amplifier Output | AD8138 Differential Output ( $V_{IN+} - V_{IN-}$ ) | AD9238 Digital Output |
|-----------------------|-------------------------------------|----------------------------------------------------|-----------------------|
| -5 V                  | -1 V                                | -1 V                                               | 000000000000          |
| 0 V                   | 0 V                                 | 0 V                                                | 100000000000          |
| +5 V                  | +1 V                                | +1 V                                               | 111111111111          |

From the table, we can see that the digital value converted by AD9238 is the smallest when -5V is input, and the digital value converted by AD9238 is the largest when it is +5V.

## Part 2.6: AN9238 Digital Output Timing

The digital output of AD9238 dual-channel AD is +3.3VCMOS output mode, 2 channels (A and B) independent data and clock. AD data converts data on the rising and falling edges of the clock, and the FPGA end can sample the AD data with the AD clock.

recoupling capacitors on REF1 and REF2.



## Part 2.7: The Pin Assignment of AN9238 Module

Only the signals of the 40-pin extension interface are listed below. For specific users, please refer to the schematic diagram

| Pin Number | Signal Name | Description    |
|------------|-------------|----------------|
| 1          | GND         | Ground         |
| 2          | +5V         | 5V Power Input |

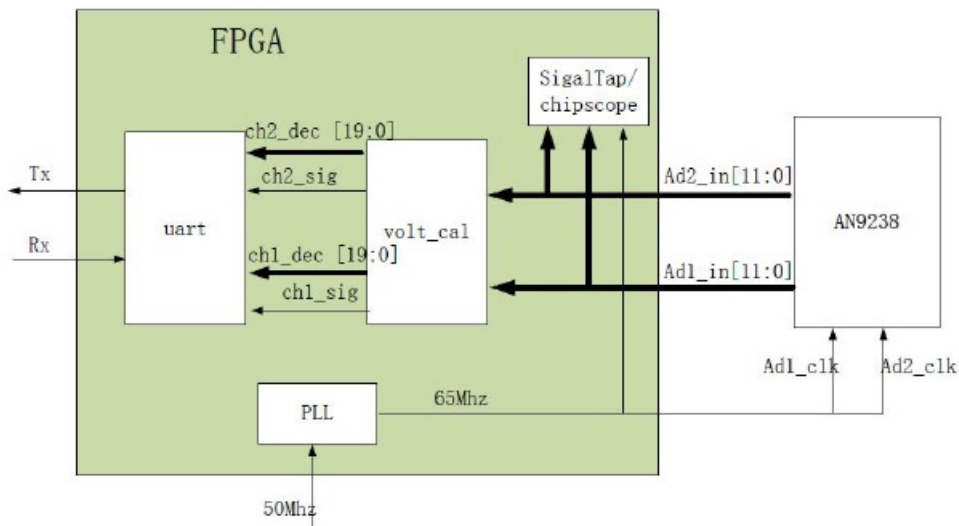
|    |         |                                             |
|----|---------|---------------------------------------------|
| 3  | CH2_CLK | AD Channel B Clock.                         |
| 4  | CH2_D0  | AD Channel B Data DATA0                     |
| 5  | CH2_D1  | AD Channel B Data DATA2                     |
| 6  | CH2_D2  | AD Channel B Data DATA2                     |
| 7  | CH2_D3  | AD Channel B Data DATA3                     |
| 8  | CH2_D4  | AD Channel B Data DATA4                     |
| 9  | CH2_D5  | AD channel B data DATA5                     |
| 10 | CH2_D6  | AD Channel B Data DATA6                     |
| 11 | CH2_D7  | AD Channel B Data DATA7                     |
| 12 | CH2_D8  | AD Channel B Data DATA8                     |
| 13 | CH2_D9  | AD Channel B Data DATA8                     |
| 14 | CH2_D10 | AD Channel B Data DATA10                    |
| 15 | CH2_D11 | AD Channel B Data DATA11                    |
| 16 | CH2_OTR | The Voltage of AD Channel B is Out of Range |
| 17 | –       | NA                                          |
| 18 | –       | NA                                          |
| 19 | CH1_D1  | AD Channel A Data DATA1                     |
| 20 | CH1_D0  | AD Channel A Data DATA0                     |
| 21 | CH1_D3  | AD Channel A Data DATA3                     |
| 22 | CH1_D2  | AD Channel A Data DATA2                     |
| 23 | CH1_D5  | AD Channel A Data DATA5                     |
| 24 | CH1_D4  | AD Channel A Data DATA4                     |
| 25 | CH1_D7  | AD Channel A Data DATA7                     |
| 26 | CH1_D6  | AD Channel A Data DATA6                     |
| 27 | CH1_D9  | AD Channel A Data DATA9                     |
| 28 | CH1_D8  | AD Channel A Data DATA8                     |
| 29 | CH1_D11 | AD Channel A Data DATA11                    |
| 30 | CH1_D10 | AD Channel A Data DATA10                    |
| 31 | CH1_CLK | AD Channel A Clock                          |
| 32 | CH1_OTR | The Voltage of AD channel A is Out of Range |
| 33 | –       | NA                                          |
| 34 | –       | NA                                          |

|    |     |        |
|----|-----|--------|
| 35 | –   | NA     |
| 36 | –   | NA     |
| 37 | GND | Ground |
| 38 | GND | Ground |
| 39 | –   | NA     |

### Part 3: AD Sampling DEMO Program Description

The program dynamically displays the waveform generated by the signal generator to the software Signaltap (chipscope), and also sends the data collected by AD to the serial port regularly, and the serial debugging tool on the computer displays the actual collected AD data value.

The whole program contains a top-level module ad9238\_test.v and three sub-modules: AD conversion module (ad.v), data conversion module (volt\_cal.v), serial port sending program (uart.v). The AD conversion module ad.v completes the collection of AD data; the data conversion module volt\_cal.v completes the voltage and hexadecimal to decimal format conversion; the serial port sending program uart.v completes the serial data transmission of the ASIC code of the collected data.



Here is a brief introduction to the functions of each module used in the FPGA program:

#### 1. volt\_cal.v

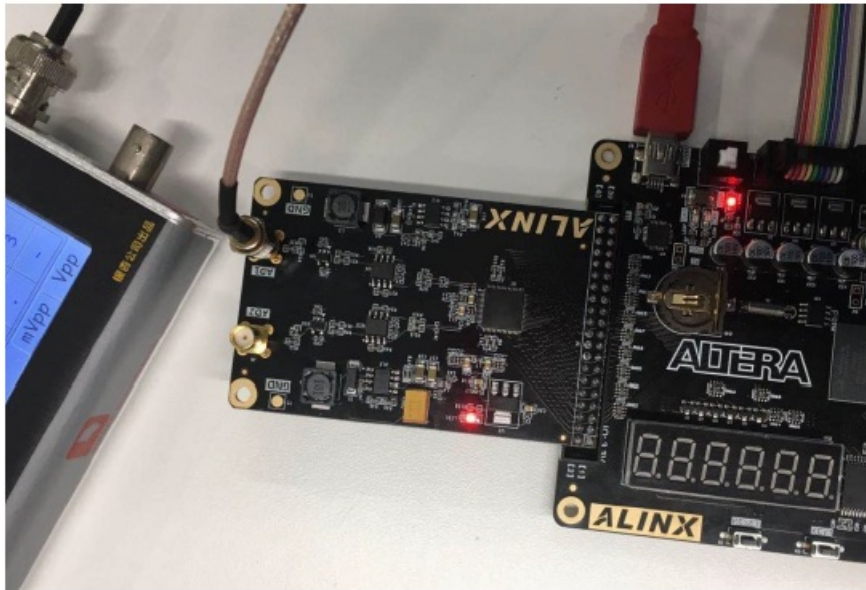
The function of the data conversion module is to convert the 12-bit data collected by the AD module into 20-bit decimal voltage data. The high bit of the 12-bit data collected by the AD module is the positive and negative sign bit. When calculating the voltage, you need to remove the high sign bit first, and then convert the remaining 11-bit data into a voltage value. The bcd.v program converts 16-digit hexadecimal data into 20-digit decimal data.

#### 2. uart.v

The serial port transmitting program regularly transmits 26 characters to the serial port to display the voltage value of channel 1 and channel 2. When the serial port transmits the decimal voltage value, it needs to be converted into ASCII code. In the program, the serial port transmitting program and the serial port clock generation program are called, and the voltage value is transmitted to the PC upper computer according to the baud rate of 9600.

## Part 4: Hardware Connection and Testing

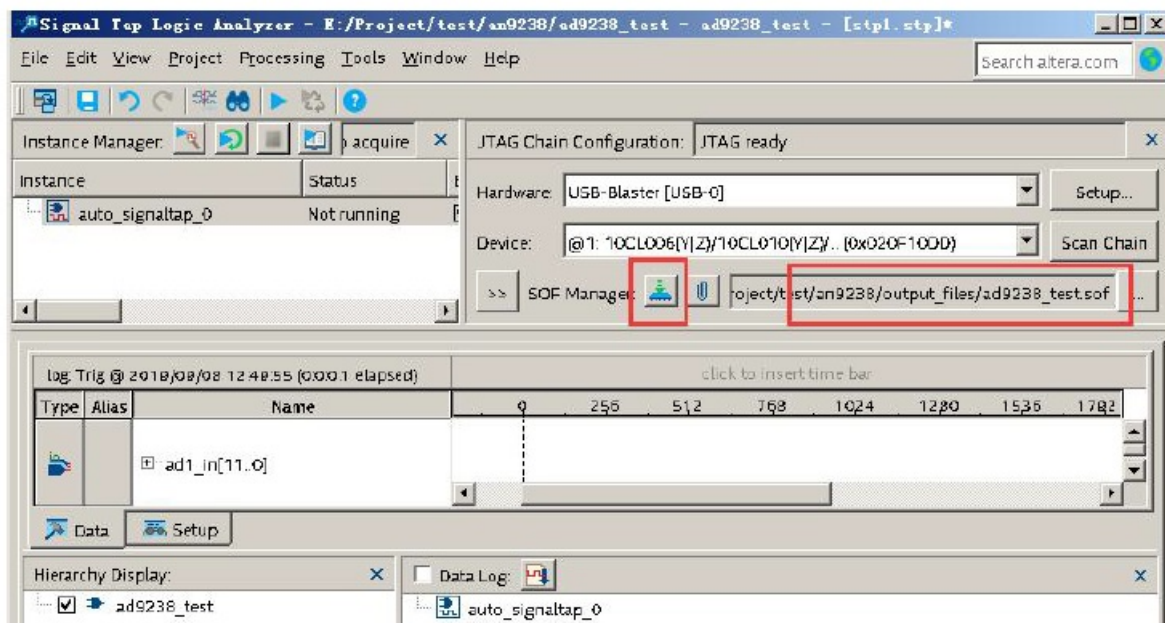
The hardware connection between AN9328 module and FPGA development board is very simple, just plug the 40-pin interface with the expansion port of the development board (AX301B/AX4010 connect to J1 port, AX309 connect to J3). The following is the hardware connection diagram of ALINX AX301B FPGA development board and AN9328:



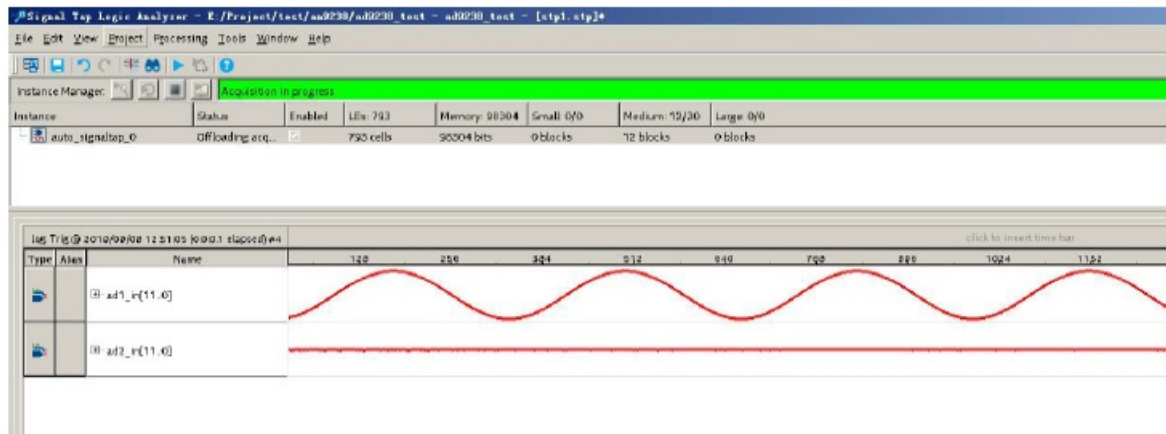
The FPGA development board is powered on, and the signal generator generates a positive wave of -5V~+5V with a frequency of 200Khz.

### Part 4.1: Take the AX301B Development Board as an example

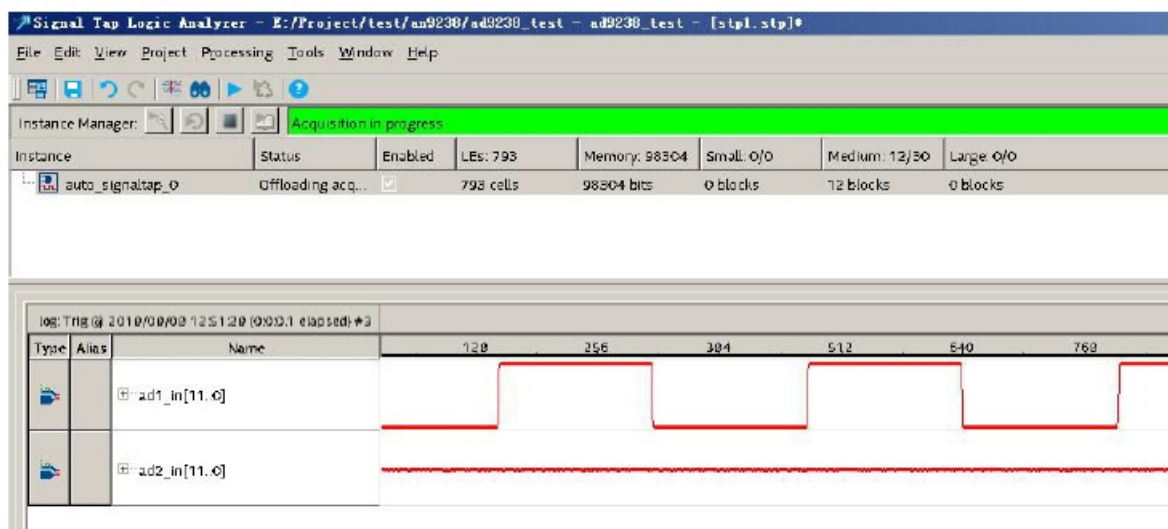
Open “signaltap” in the Quartus software and download the “ad9238\_test.sof” file.



After downloading, run signaltap, the waveform interface will display a positive wave signal



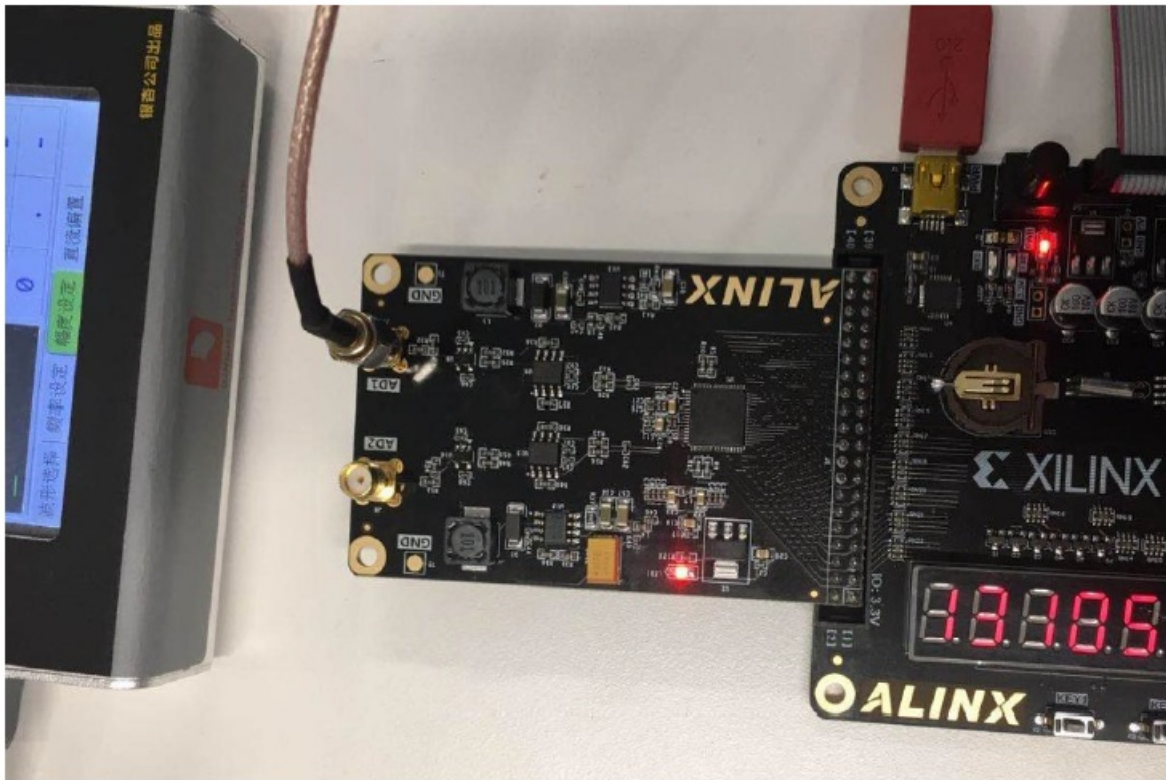
Change the signal transmitter to generate a square wave of -5V~+5V, and the ad channel will display a square wave.



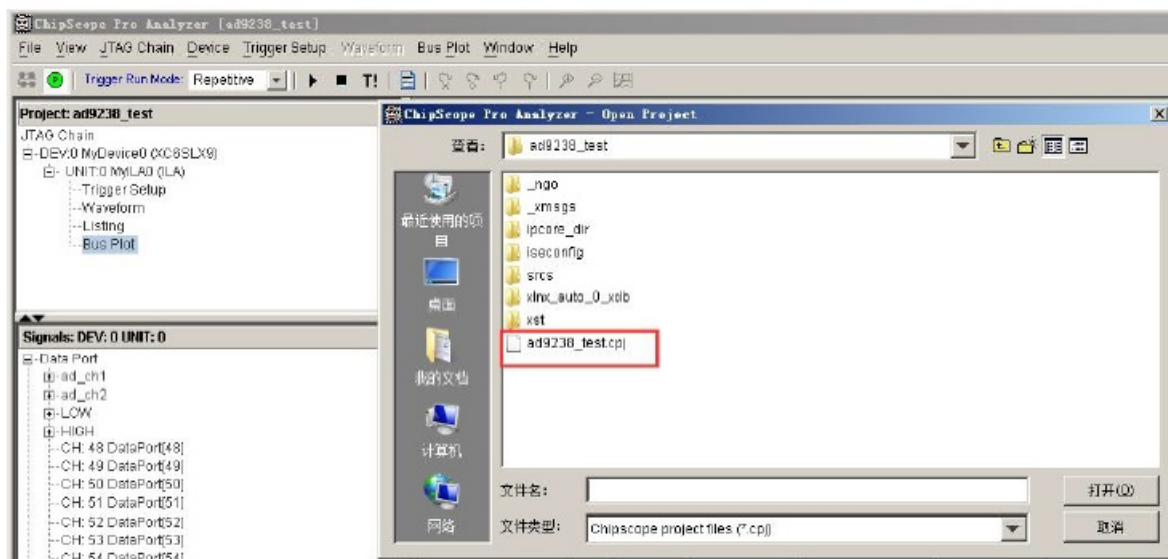
Here we can observe the signal in hexadecimal, set it to hexadecimal and display as follows.

#### Part 4.2: Take the AX309 Development Board as an example

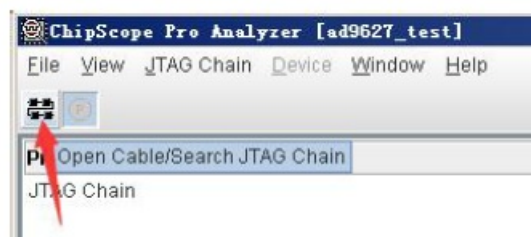
The following is the hardware connection diagram of ALINX AX309 FPGA development board and AN9328:



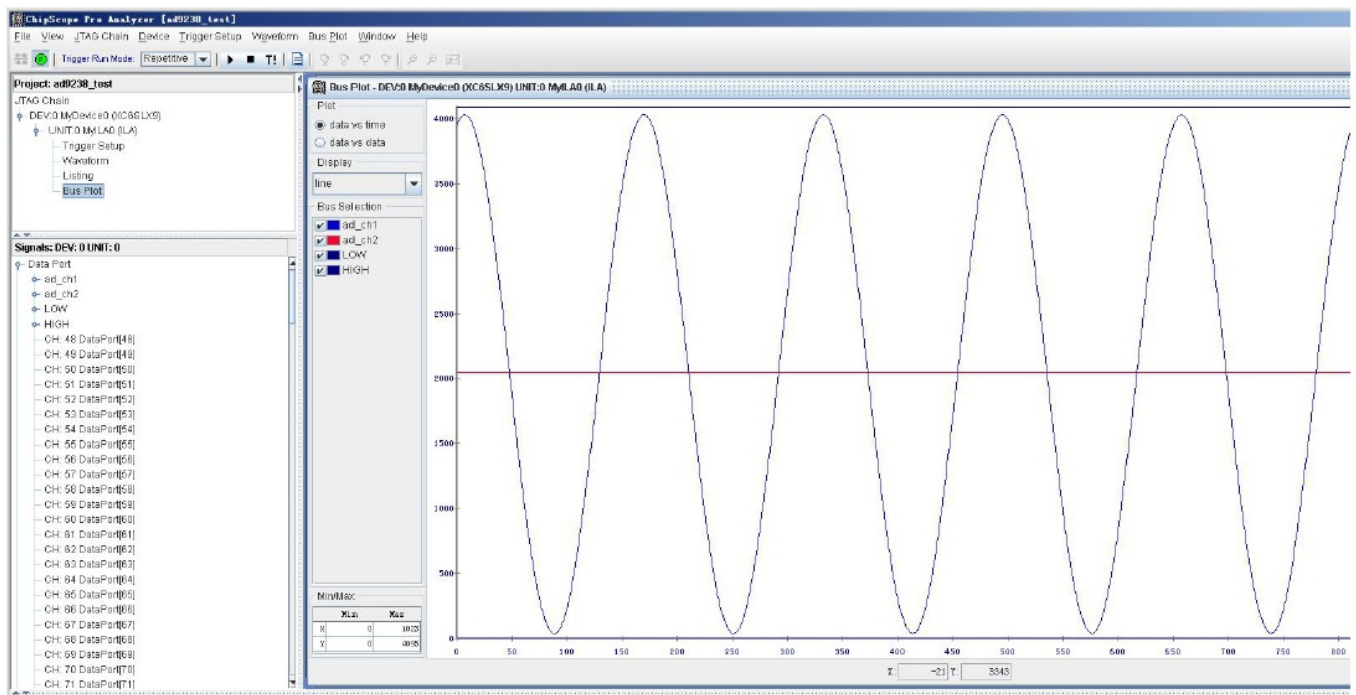
Download the “ad9238\_test.bit” file in the Impact software, then open the “chipscope” software, and open the “ad9238\_test.cpj” project in the chipscope.



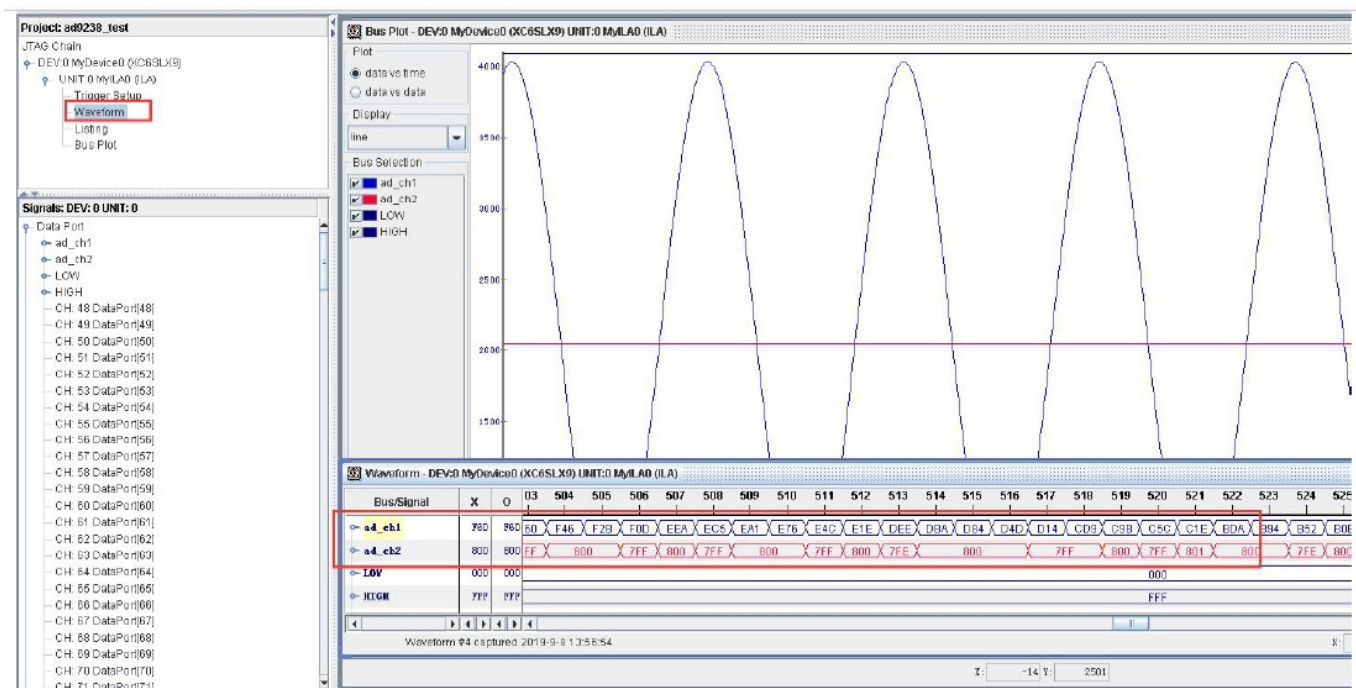
Click the “Open Cable/Search JTAG Chain” button to connect to the FPGA development board



Open the “Bus Plot” interface, and the waveform interface will display a sine wave signal.

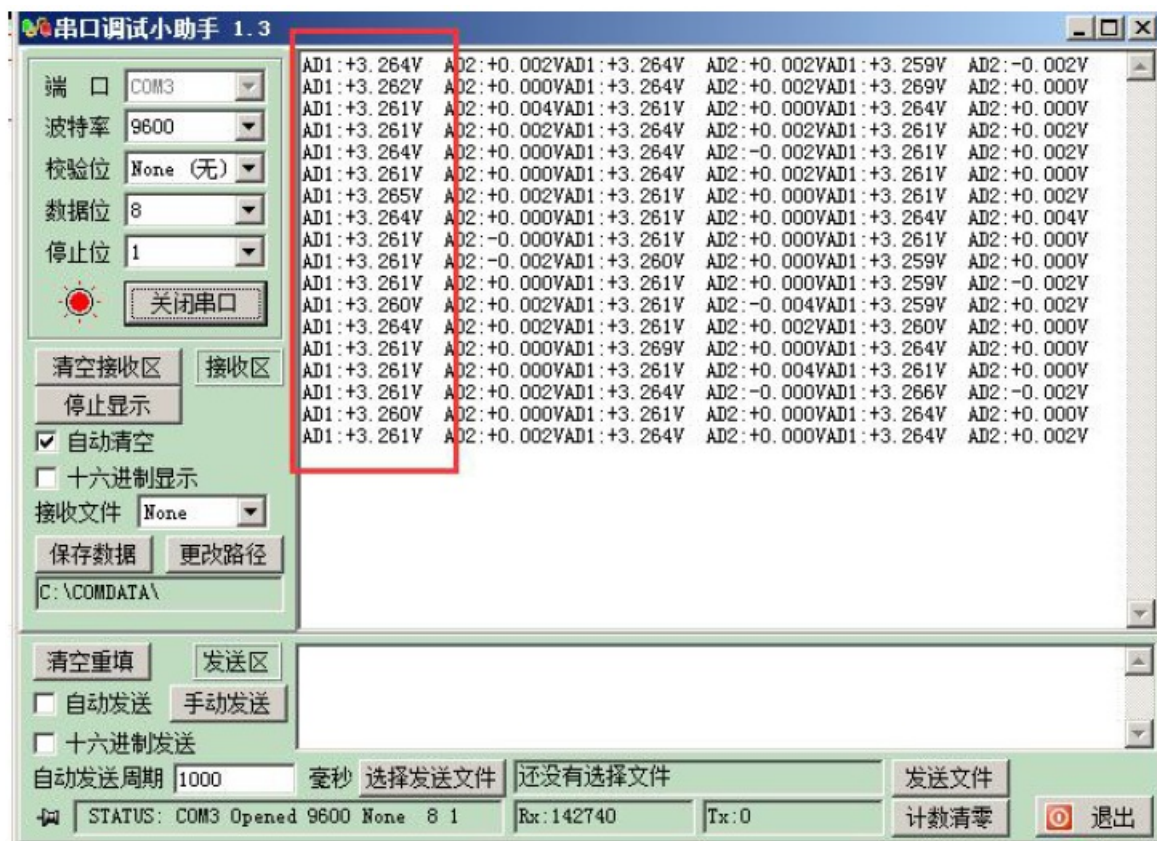


The specific data (hexadecimal data) sampled by AD is displayed in the waveform window.



### Part 4.3 Serial Display Voltage

In addition, we can see the converted voltage value through the serial port, and the baud rate of the serial port is set to 9600. For example, AD input DC voltage +3.3V, the display is as follows (different modules will have certain deviations).



When the DC voltage is changed to -3.3V, the display is as follows (different modules will have certain deviations).



|                                                                                       |                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <div>2-Channel High Speed<br/>AD Module AN8238<br/>User Manual</div> <div>ALINX</div> | <div><a href="#">ALINX AN8238 2 Channel High Speed AD Module</a> [pdf] User Manual</div> <div>AN8238, 2 Channel High Speed AD Module, AN8238 2 Channel High Speed AD Module, High Speed AD Module, AD Module, Module</div> |
|---------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

References

-  [ALINX](#)