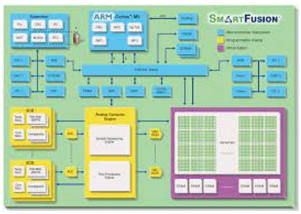

Actel SmartFusion Microcontroller Subsystem (MSS) User Guide

SmartDesign MSS
Ethernet MAC Configuration

Contents

Introduction

The SmartFusion Microcontroller Subsystem (MSS) provides one Ethernet MAC hard peripheral. The actual behavior of the Ethernet MAC must be defined at the application level using the SmartFusion MSS MAC Driver provided by Actel.
In this document, we describe how you can enable the MSS MAC instance and select whether the Ethernet MAC interface is connected to dedicated MSS I/Os or the FPGA fabric.
For more details about the MSS MAC hard peripheral, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Configuration Options

Enabling/Disabling the MAC Instance. On the MSS canvas, you need to enable (default) or disable the MAC

instance based on whether it is being used into your current application. If disabled, the MAC instance is held in reset (lowest power state) after the Actel system boot code is executed.

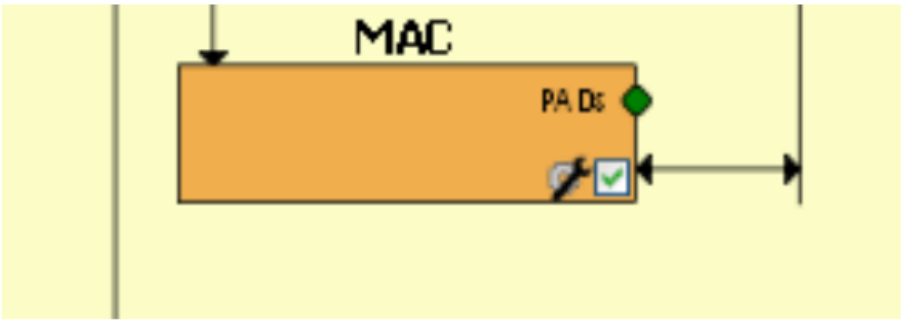

Figure 1: MSS MAC Configurator

Connectivity Options. When using the A2F200M3F device, the Ethernet MAC, when enabled, can only be connected to dedicated MSS I/Os. When using the A2F500M3G device, you can choose to connect the MAC peripheral to dedicated MSS I/Os or the FPGA fabric. In all cases, the MAC connectivity is automatically configured by the Actel system boot code. Note that MSS I/Os allocated to the MAC instance are available to connect to the FPGA fabric if the MAC instance is disabled. Refer to the MSS I/O Configuration document for more details. To use the MAC FPGA ports (if that option is selected), you need to manually promote to the top level the FABRIC group port present on the MSS MAC instance. You can then use the FABRIC MAC ports in the next level of hierarchy.

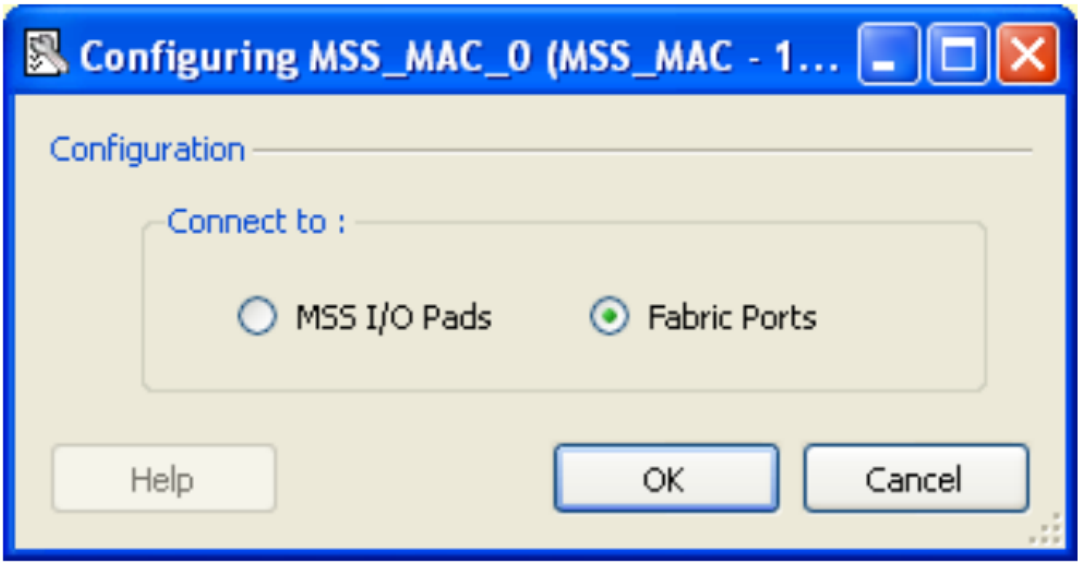

Figure 2: MSS MAC Configuration Options

Ethernet MAC Clock Selection. If you enable the MAC peripheral on the MSS configurator canvas the MAC clock is automatically selected (read-only) in the Clock configurator. Using the MSS Clock configurator you need to select one of the following MAC clock sources.

- The external 10/100 clock (MAC_CLK pin) on the SmartFusion device.
- A clock generated in the MSS Clock Conditioning Circuit (MSS_CCC).

Port Description

Table 1: MSS I/O Connectivity Options

Port Name	Port Group	Direction	PAD?	Description
RXER	PADs	In	Yes	Receive error. If RX_ER is asserted during Ethernet MAC reception, the frame is received and status of the frame is updated with RX_ER.
CRSDV	PADs	In	Yes	Carrier sense and receive data valid. This signal must be asserted by the PHY when either a receive or transmit medium is non-idle. The PHY device should assert MAC_CRSDV when valid data is provided on the RXD signal.
MDIO	PADs	Inout	Yes	RMII management data input and output. The state of the input signal can be checked by reading the CSR9.19 bit. The output signal is driven by the CSR9.18 bit.
RXD[1:0]	PADs	In	Yes	Receive data recovered and decoded by PHY. The RXD[0] signal is the least significant bit.
TXEN	PADs	Out	Yes	Transmit enable. When asserted, indicates valid data for the PHY on the TXD port.
MDC	PADs	Out	Yes	RMII management clock = 25 MHz. This signal is driven by the CSR9.16 bit.
TXD[1:0]	PADs	Out	Yes	Transmit data. The TXD[0] signal is the least significant bit.

Table 2: FPGA Fabric Connectivity Options

Port Name	Port Group	Direction	PAD?	Description
F2M_RXER	FABRIC	In	No	Receive error. If RX_ER is asserted during Ethernet MAC reception, the frame is received and status of the frame is updated with RX_ER.
F2M_CRSDV	FABRIC	In	No	Carrier sense and receive data valid. This signal must be asserted by the PHY when either a receive or transmit medium is non-idle. The PHY device should assert MAC_CRSDV when valid data is provided on the RXD signal.
F2M_MDI	FABRIC	In	No	RMII management data input. The state of the input signal can be checked by reading the CSR 9.19 bit

Port Name	Port Group	Direction	PAD?	Description
M2F_MDIO	FABRIC	Out	No	RMII management data output. The output signal is driven by the CSR9.18 bit.
M2F_MDEN	FABRIC	Out	No	RMII management data output enable.
F2M_RXD[1:0]	FABRIC	In	No	Receive data recovered and decoded by PHY. The RXD[0] signal is the least significant bit.
M2F_TXEN	FABRIC	Out	No	Transmit enable. When asserted, indicates valid data for the PHY on the TXD port.
M2F_MDC	FABRIC	Out	No	RMII management clock = 25 MHz. This signal is driven by the CSR9.16 bit.
M2F_TXD[1:0]	FABRIC	Out	No	Transmit data. The TXD[0] signal is the least significant bit.

Notes:

- PAD ports are automatically promoted to top throughout the design hierarchy.
- Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.

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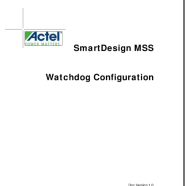	**Actel SmartFusion Microcontroller Subsystem (MSS)** [pdf] User Guide SmartFusion Microcontroller Subsystem MSS

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