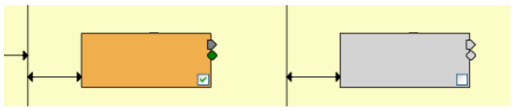

Actel SmartDesign MSS SPI Configuration User Guide

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Introduction

The SmartFusion Microcontroller Subsystem (MSS) provides two SPI hard peripherals (APB_0 and APB_1 sub busses) with optional FPGA fabric slave select ports extension.
The actual behavior of each SPI instance must be defined at the application level using the SmartFusion MSS SPI Driver provided by Actel.
In this document, we describe how you can enable the MSS SPI instances and access the fabric slave select ports. For more details about the MSS SPI hard peripherals, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.

Configuration Options

Enabling/Disabling SPI Instances. On the MSS canvas, you need to enable (default) or disable each SPI instance

based on whether it is being used in your current application. Disabled SPI instances are held in reset (lowest power state) after the Actel system boot code is executed. Enabled SPI instances external ports – MSS I/Os – are also automatically configured by the Actel system boot code. Note that MSS I/Os allocated to a SPI instance are available to connect to MSS GPIOs if that SPI instance is disabled. Refer to the **MSS GPIO** configurator handbook for more details.

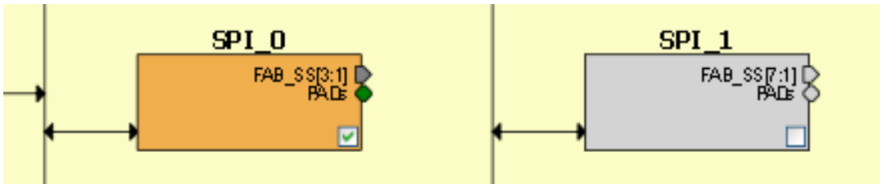

Figure 1: MSS SPI

Fabric Slave Select Extension. You may drive up to 3 slave select signals for SPI_0 and 7 for SPI_1 into the FPGA fabric; to do this, you need to manually promote to the top level the FAB_SS[] port present on the MSS SPI instance(s) used in your application. You can then use the FAB_SS port in the next level of hierarchy where it can be 'sliced' as individual slave select signals.

Port Description

Port Name	Port Group	Direction	PAD?	Description
DI	PADs	In	Yes	Shift data in (master or slave)
DO	PADs	Out	Yes	Serial data out (generated by SPI as master)
CLK	PADs	Inout	Yes	Shift clock out (generated by SPI as master)
SS	PADs	Inout	Yes	External dedicated slave select port (generated by SPI as master)
FAB_SS[n:1]		Out	No	Optional routed slave select ports (generated by SPI as master)

Notes:

- PAD ports are automatically promoted to top throughout the design hierarchy.
- Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.

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Documents / Resources

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