



Actel SmartDesign MSS Cortex M3 Configuration User Guide

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SmartDesign MSS Cortex™ -M3 Configuration User Guide

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Introduction

The SmartFusion Microcontroller Subsystem (MSS) contains an ARM Cortex-M3 microcontroller, a lowpower processor that features low gate count, low and predictable interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features.

This document describes the ports that are available on the Cortex-M3 core in the SmartDesign MSS Configurator.

For more information about the specific implementation of the Cortex-M3 in the Actel SmartFusion device, please refer to the [Actel SmartFusion Microcontroller Subsystem User's Guide](#).

Configuration Options

There are no configuration options for the Cortex-M3 core in the SmartDesign MSS Configurator.

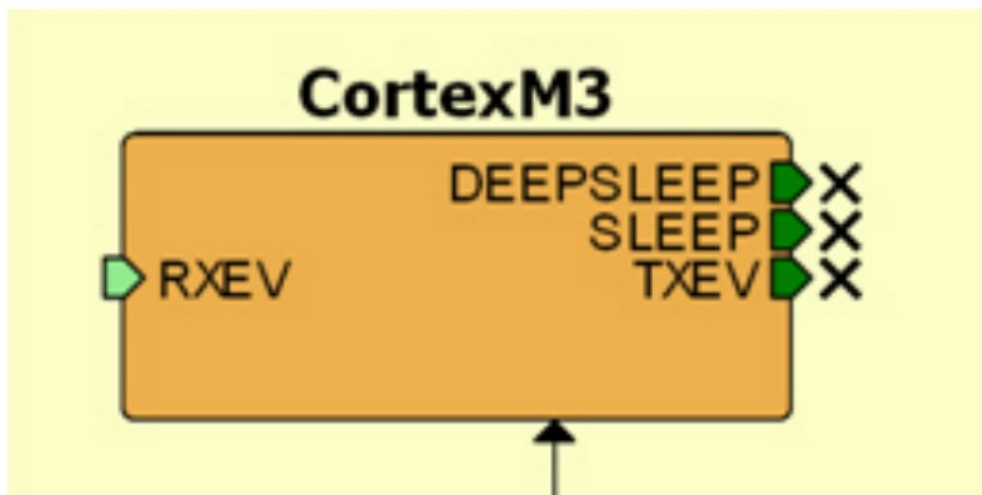


Figure 1: Cortex-M3 in SmartFusion

Port Description

Port Name	Direction	PAD?	Description
RXEV	In	No	Causes the Cortex-M3 to wake up from a WFE (wait for event) instruction. The event input, RXEV, is registered even when not waiting for an event, and so affects the next WFE.
TXEV	Out	No	Event transmitted as a result of a Cortex-M3 SEV (send event) instruction. This is a single-cycle pulse equal to 1 FCLK period.
SLEEP	Out	No	This signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode, and indicates that the clock to the processor can be stopped.
DEEPSLEEP	Out	No	This signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode when the SLEEPDEEP bit of the System Control Register is set.

Note:

Non-PAD ports must be promoted manually to the top level from the MSS configurator canvas to be available as the next level of hierarchy.

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Documents / Resources

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References

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