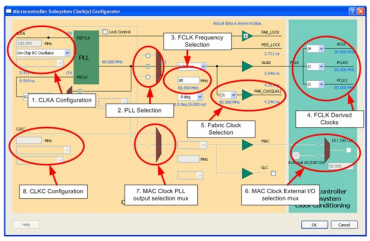

Actel Smart Design MSS Clock Configuration User Guide

SmartDesign MSS
Clock Configuration

Contents

Introduction

The Clock Management Configurator provides a single place where all clocks related to the MSS and the communication between the MSS and the FPGA fabric can be configured. For a complete description of the SmartFusion device clocking scheme, please refer to the Actel SmartFusion Microcontroller Subsystem User's Guide.
The MSS Clock Conditioning Circuitry (MSS_CCC) is configured by the Actel System Boot code based on the selection made in this configurator.

Configuration Options

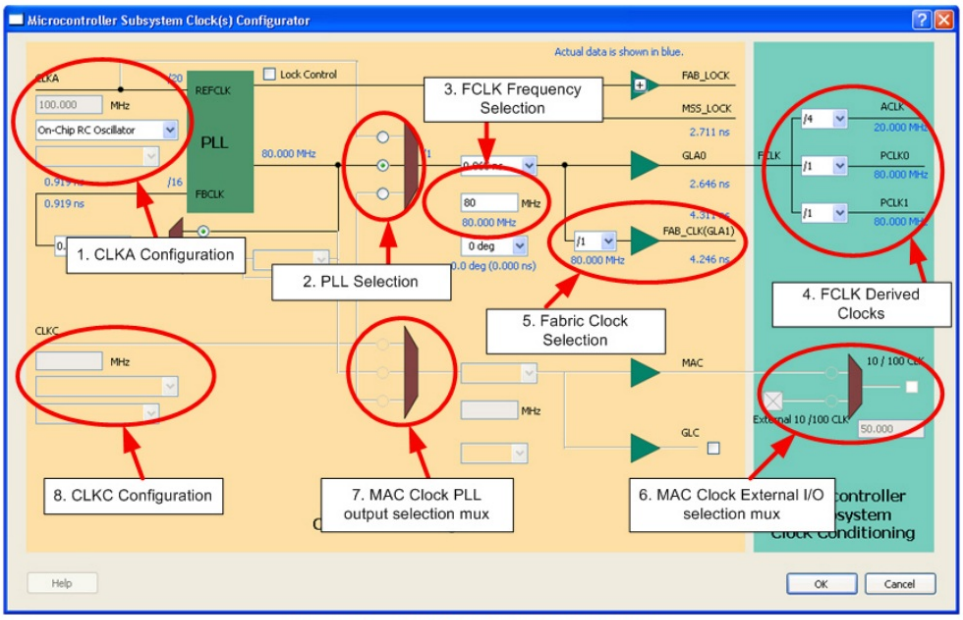

Figure 1: MSS CCC Configuration Options

CLKA Reference Clock

To configure the CLKA reference clock, first select the clock source, then define the clock source frequency and, in the case of the hardwired I/O sources, the package pin assignment.

- Clock Source Selection. The following sources are available from the reference clock pull-down menu:

  – External I/O. The clock source can be any fabric I/O. The fabric I/O is routed to the reference clock fabric interface pin.

  – Hardwired I/O. The clock source is one of three fabric I/Os that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKA pin when choosing this option (see the Clock Pin Assignment option for more details).

  – Hardwired I/O (LVPECL). The clock source is one of two fabric I/Os (P side of the LVPECL pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKA pin when choosing this option (see the Clock Pin Assignment option for more details).

  – Hardwired IO (LVDS). The clock source is one of two fabric I/Os (P side of the LVDS pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKA pin when choosing this option (see the Clock Pin Assignment option for more details).

  – Internal logic. The clock source can be any FPGA fabric logic.

  – On-chip RC Oscillator. The clock source is a dedicated 100 MHz On-chip RC Oscillator available on the SmartFusion device.

  – Main Crystal Oscillator. The source is an external Crystal. See the Actel SmartFusion Microcontroller Subsystem User's Guide for details about how the external crystal must be connected on the board to the SmartFusion device.

  – Main Crystal Oscillator (RC network). The source is an external RC circuit connected to the main crystal oscillator external pins. See the Actel SmartFusion Microcontroller Subsystem User's Guide for details about how the external RC network must be connected on the board to the SmartFusion device.

- Clock Frequency. You must specify the clock source frequency. Note the following frequency requirements:

  – The On-chip Oscillator clock frequency is fixed to 100 MHz and cannot be changed.

  – The Main Crystal Oscillator clock frequency must be between 1.5 MHz and 20 MHz when the PLL is used or between 32 KHz and 20 MHz when the PLL is bypassed.

  – The Main Crystal Oscillator (RC network configuration) clock frequency must be between 1.5 MHz and 4 MHz

when the PLL is used or between 32 KHz and 4 MHz when the PLL is bypassed.

– For all other sources, the source clock frequency must be between 1.5 MHz and 176MHz when the PLL is used or between 32 KHz and 250 MHz when the PLL is bypassed.

- Clock Pin Assignment. When choosing a hardwired I/O option you must select a package pin assignment for the reference clock port. The pin assignment list may be different based on the hardwired I/O option chosen as well as the package selected for the current design. Note the following pin assignment requirements:

  – If the External Memory Controller (EMC) has been enabled in the design, the LVDS option is not available. This is due to the fact that the EMC I/Os are placed in the same bank as the I/Os that have a dedicated connection to the reference clock CLKA. The EMC I/Os are using the LVTTL (3.3V) standard which is not compatible with LVDS (2.5V).

  – If the reference clock CLKC is used and uses a hardwired option, it must be compatible with the CLKA selection (i.e. LVDS and LVPECL are not compatible).

FCLK (GLA0) Clock

To achieve the desired the MSS clock (FCLK) frequency, you may need to select the use of the PLL component. The actual frequency is displayed in blue below the frequency edit box. The following sources are available from the reference clock pull-down menu:

- PLL Bypass. To use this option, select the first button for the PLL selection radio button.
- VCO (0, 90, 180 and 270 degrees). To use this option, select the second button for the PLL selection radio button and select the phase using the phase selection pull-down menu.
- VCO (0 degree) with programmable delay. To use this option, select the third button for the PLL selection radio button.

FCLK Derived Clocks

There are three internal APB sub-busses in the MSS – ACE, APB sub-bus 1 and 2 -. Each of these subbusses peripherals are clocked by a derived clock from the MSS clock (FCLK). Each derived clock can be programmed individually as FCLK divided by 1, 2 or 4.

Note that some peripherals may require a slower PCLK to achieve certain configurations. Changing the PCLK of a sub-bus affects all peripherals present on that bus. For more details, please refer to the **Actel SmartFusion Microcontroller Subsystem User's Guide**.

Fabric Clock (FAB_CLK)

For applications where the AMBA fabric extension is used to connect to a soft AMBA subsystem (soft bus/bridge/peripheral cores), the fabric clock (FAB_CLK) must be configured such that the generated frequency meets the timing requirements of the logic implemented in the fabric. The fabric clock, when used, can only be the MSS clock divided by 1, 2 or 4 as per the architecture requirements for the SmartFusion device. You need to verify that the fabric timing meets the selected fabric clock frequency by performing timing analysis of their design using SmartTime.

Ethernet MAC Clock

If you enable the MAC peripheral on the MSS configurator canvas the MAC clock is automatically selected (read-only) in the Clock configurator. You also need to define the MAC clock source as one of the two following options:

- The external 10/100 clock on the SmartFusion device.
- A clock generated in the MSS Clock Conditioning Circuit (MCCC). In this case, the clock can either be:

  – Derived from the MSS reference clock using the PLL component output.

  – Selected from one of the following reference clock (CLKC) pull-down menu sources (see CLKC Reference Clock).

GLC Clock

You may optionally enable the GLC clock. The GLC clock drives a global network in the FPGA fabric. The source of the GLC clock can either be:

- Derived from the MSS reference clock using the PLL component output.
- Selected from one of the following reference clock (CLKC) pull-down menu sources (see CLKC Reference Clock)

Note that the source of the GLC clock is the same as the MAC clock source if the MAC clock is generated from the MSSS CCC.

CLKC Reference Clock

To configure the CLKC reference clock, first select the clock source, then define the clock source frequency and, in the case of the hardwired I/O sources, the package pin assignment.

- Clock Source Selection. The following sources are available from the reference clock pull-down menu:
  – External I/O. The clock source can be any fabric I/O. The fabric I/O is routed to the reference clock fabric interface pin.
  – Hardwired I/O. The clock source is one of three fabric I/Os that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKC pin when choosing this option (see the Clock Pin Assignment option for more details).
  – Hardwired I/O (LVPECL). The clock source is one of two fabric I/Os (P side of the LVPECL pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKC pin when choosing this option (see the Clock Pin Assignment option for more details).
  – Hardwired I/O (LVDS). The clock source is one of two fabric I/Os (P side of the LVDS pair) that has a dedicated path to drive the reference clock. You must select a package pin assignment for the CLKC pin when choosing this option (see the Clock Pin Assignment option for more details).
  – Internal logic. The clock source can be any FPGA fabric logic.
  – On-chip RC Oscillator. The clock source is a dedicated 100 MHz On-chip RC Oscillator available on the SmartFusion device.
  – Low Power 32 KHz Crystal Oscillator. The source is the same Low Power Crystal Oscillator (32 KHz) that drives the RTC block. See the Actel SmartFusion Datasheet for details about how the external crystal must be connected on the board to the SmartFusion device.
- Clock Frequency. You must specify the clock source frequency. Note the following frequency requirements:
  – The On-chip Oscillator clock frequency is fixed to 100 MHz and cannot be changed. – The Low Power Crystal Oscillator clock frequency is fixed to 32 KHz and cannot be changed. For all other sources, the source clock frequency must be between 32 KHz and 250 MHz.
- Clock Pin Assignment. When choosing a hardwired IO option you must select a package pin assignment. The pin assignment list may be different based on the hardwired IO option chosen as well as the package selected for the current design. Note the following pin assignment requirements:
  – If the EMC has been enabled in the design, the LVDS option is not available. This is due to the fact that the EMC I/Os are placed in the same bank as the I/Os that have a dedicated connection to the reference clock CLKC. The EMC I/Os are using the LVTTL (3.3V) standard which is not compatible with LVDS (2.5V).
  – If the reference clock CLKA is used and uses a hardwired option, it must be compatible with the CLKC selection (i.e. LVDS and LVPECL are not compatible).

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Documents / Resources

	Actel Smart Design MSS Clock Configuration [pdf] User Guide Smart Design MSS Clock Configuration, Smart Design MSS, Clock Configuration

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