ST EEPROM Cycling and Data Retention Performances User Guide

Contents

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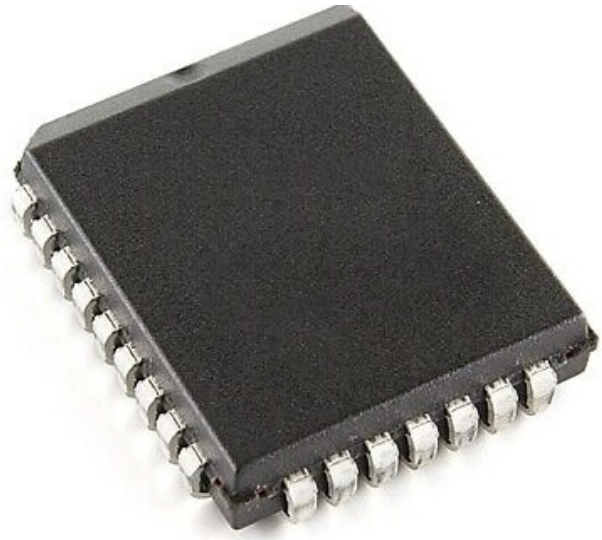


Introduction

This application note details the ST page EEPROM cycling and data retention performances. Reliability and endurance are key requirements for datalogging or event recording applications. A very high level of quality is consequently mandatory for these electronic applications. This application note applies to the Page EEPROMs products listed in Table 1.

Applicable products

Root part number reference	Commercial Part Numbers
M95P16-I	M95P16-xxxxx
M95P16-E	M95P16-xxxxx
M95P32-I	M95P32-xxxxx
M95P32-E	M95P32-xxxxx

Page EEPROM cycling performance

Cycling budget

Page EEPROMs can write data with:

- Page Program operation that needs erased bytes (FFh) to program data
- Page Write operation that is a Page Erased followed by a Page Program operation

For more information about Page Program and Page Write operations refer to the application note AN5747 (Page EEPROM memory architecture).

Glossary

Parameter	Definition
Cycle	Page write operation (1 to 512 bytes) or erase operation (page, sector, block, or chip erase)
Cycling	Cumulated number of cycles

Note: One program operation executed between two erases operations does not count as a cycle.

As specified in the related datasheets, the cycling budget is 500 k per page over the full temperature and supply voltage ranges which makes page EEPROMs very flexible. This cycling budget represents the sum of page write and erase operations over a page:

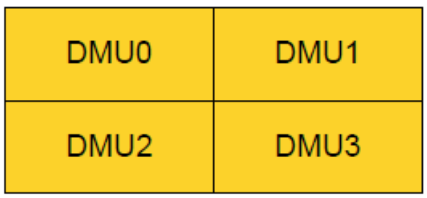
- A page write of 1 byte or a page write of 512 bytes both represent one cycle over the page.
- A page erase of 512 bytes represents one cycle over the page. Whatever the amount of page program operations.
- A sector erase (4 KB) represents one cycle for each of the 8 pages erased.
- A block erase (64 KB) represents one cycle for each of the 128 pages erased.
- A chip erase represents one cycle for each page of the memory.

The cycling budget of page EEPROM products are easy to calculate and allows byte cycling thanks to the page write operation. The error correction code (ECC) has no effect on cycling budget

For more information about ECC refer to the application note AN5747 (Page EEPROM memory architecture)

Cycling qualification method
The qualification cycling pattern is defined to reach three weeks (~ 500 h cycling time) as defined in JEDEC JESD47. During the qualification phase, the page EEPROM parts are cycled and then read to locate eventual failing bit. Page EEPROM architecture embeds DMU (data memory unit) as illustrated in the figure below

M95P32 DMU architecture



In the M95P32, each DMU are cycled from 1% (5 k cycles) to 100% max specification (500 k cycles) with different erase operations (page erase, sector erase and block erase). DMU are not cycled at the same time to check if cycling one DMU does not disturb the others. The full content is always verified with a read operation.

Overall number of cycles
The number of cycles can be defined either for each page or for the overall number of cycles decoded by the whole memory:

- **The max cycling value defined in the datasheet is the max number of cycles for each page** : 500 K cycles.
- **The overall number of cycles is the maximum number of cycles qualified for the page EEPROM:** 1 billion cycles

Page EEPROMs cycling strategies

Simple recommendations and good cycling strategy can really optimize the cycling endurance of page EEPROM products. As a power-down during a page write cycle can corrupt the whole addressed page, the areas containing the read-only parameters and the cycled items should be separated and made as much as possible independent from each other. These two types of data should not share the same pages.For more information about power loss and data corruption refer to the application note AN5747 (Page EEPROM memory architecture). Also, it is recommended to gather data which have the same cycling rates. These gathered data is called data class in the following cycling strategies.

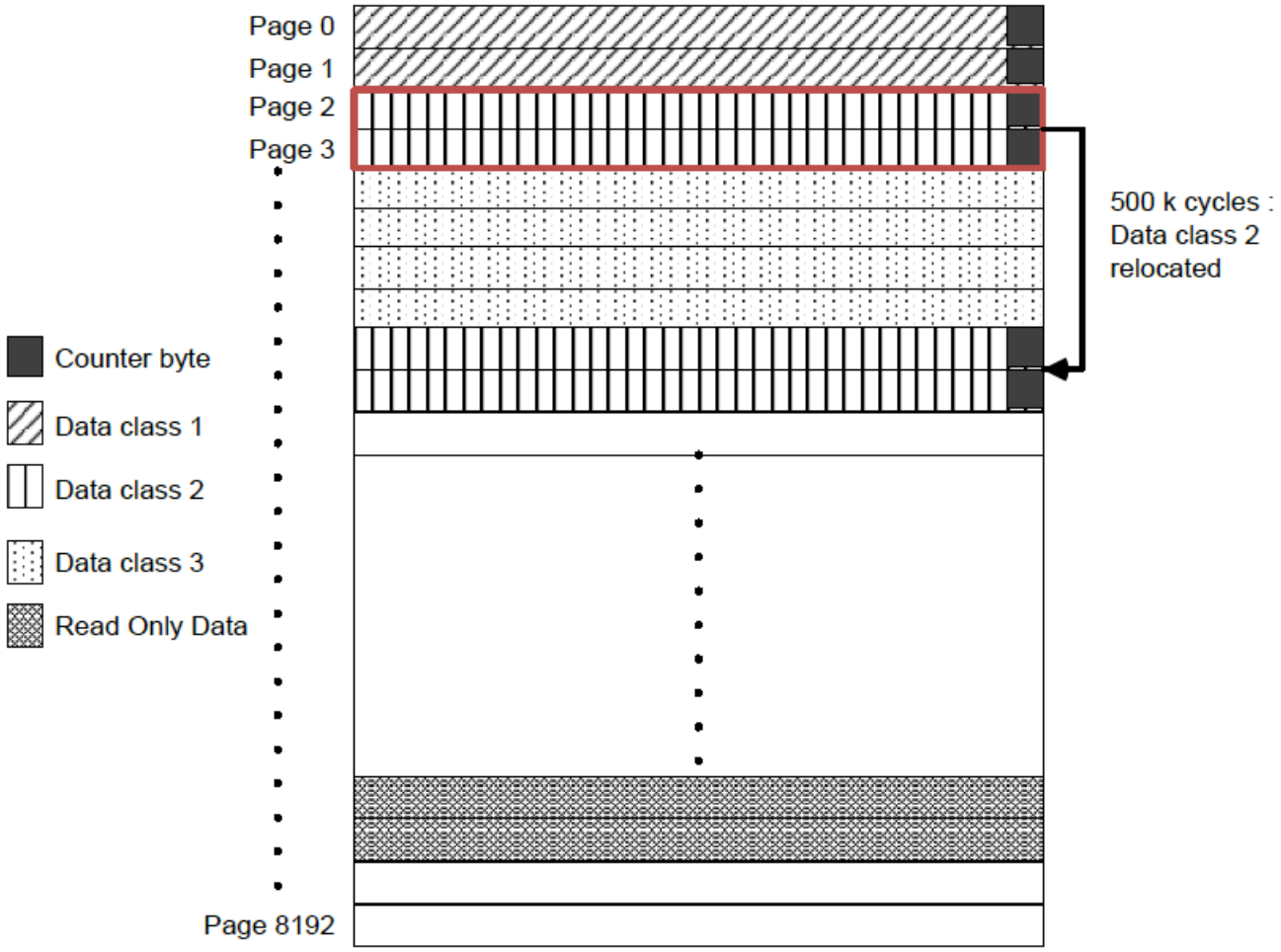
Page EEPROM strategy 1: pages counting cycling strategy

The first cycling strategy is monitoring the write endurance of each page with a dedicated counter byte. With data class and page counter value, if one page reaches the 500k cycles the whole data class should be relocated to another physically independent memory address.

Example:

In Figure 2, data class 1 cycles every hour and data class 2 cycles every minute. If one page of Data class 2 reached 500 k cycles, the whole data class (page 3 + page 4) is relocated further in the memory array as show in Figure 1. The read only pages and the data classes stay separated

Page EEPROM pages counting cycling strategy



Page EEPROM strategy 2: data class budget

The second cycling strategy recommends the designer to allocate enough memory for a data class. The memory allocated is calculated with the total amount of cycles the data class realizes during the whole application lifetime. If different data class are cycled, several parts of the memory should be allocated for each data class type.

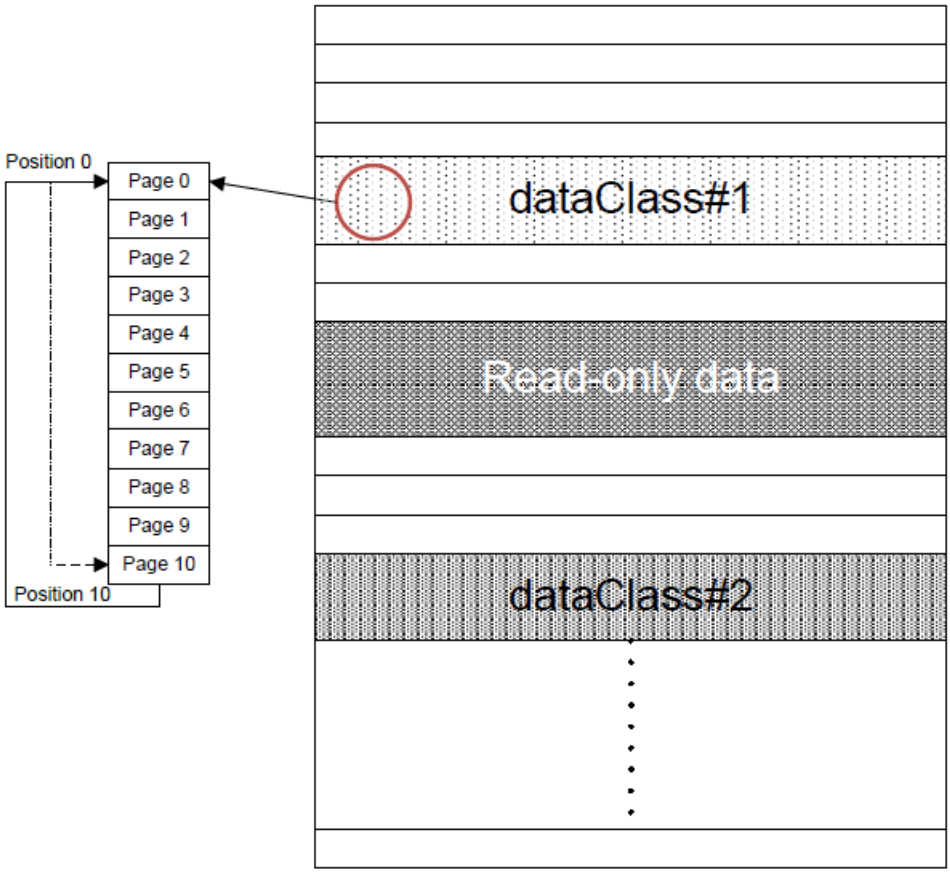
Example:
An application runs with the M95P32 page EEPROM, 32 bytes are cycled every minutes and 4 bytes every 10 minutes. The application lifetime is 10 years.

Two data class can be identified:

- **dataClass#1**: years × days × *h*ours × minutes = DataClass#1 application cycling budget 10 × 365 × 24 × 60 = 5 256 000 cycles
- **dataClass#2**: years × days × *h*ours × minutes = DataClass#2 application cycling budget 10 × 365 × 24 × 6 = 525 600 cycles

As the page cycling endurance of page EEPROM products is 500 k: dataClass#1 needs at least 11 pages to fit the 5 256 000 cycles (5 256 000 500 000), which represents 478 182 cycles per page dataClass#2 needs at least 2 pages to fit the 525 600 cycles (525 600 500 000), which represents 262 800 cycles per page The following figures show how these data class can be allocated in a 32 Mbit page EEPROM..

Cycling Strategy with data class budget



The cycle begins at pointer position 0. Each cycle, the pointer is incremented to write the next page. When the last page is reached, the position is reset. So, the 11 pages are cycled 478182 times. This strategy has the benefit of distributing the cycling over several locations and avoid max stress on a same area.

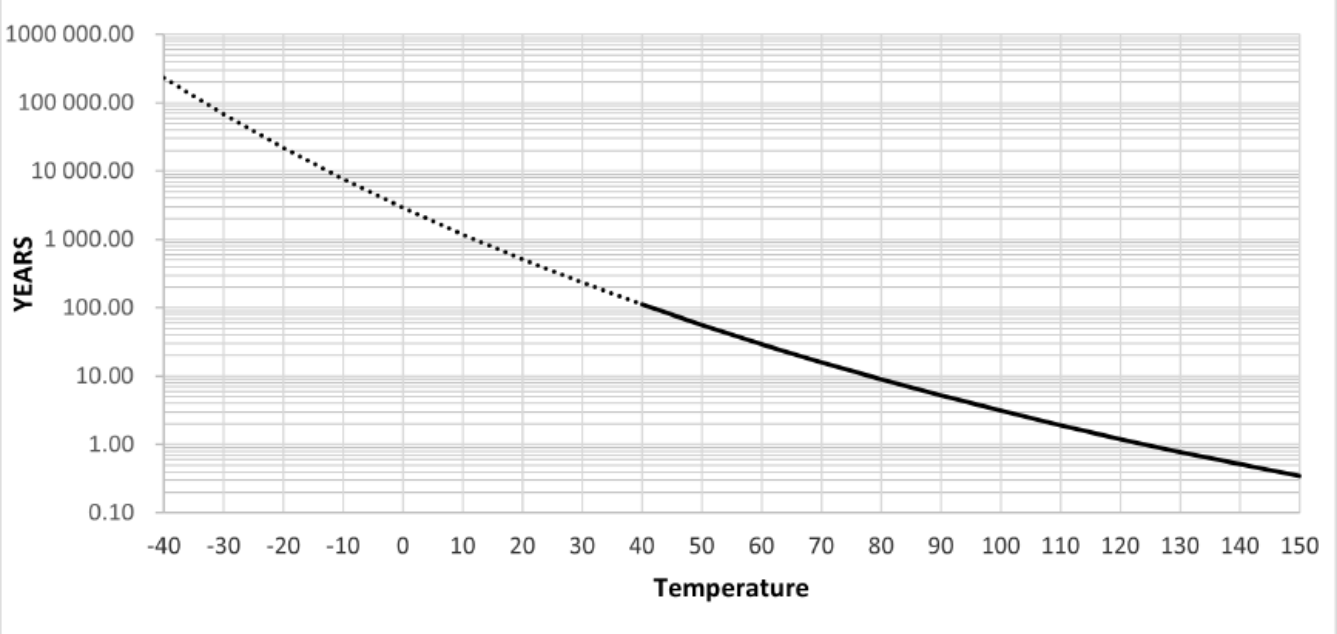
Page EEPROM data retention

Definition
At t0, bytes are written, after what no page write or erase operations are executed on these bytes. The data retention time is the time after t0 during which the bytes can still be correctly read (the page EEPROM devices being DC supplied or not).

Data retention and temperature dependence
Page EEPROMs data retention is temperature dependent. The higher is the temperature the lower is the data retention time. The next figures show the data retention compared to the temperature for

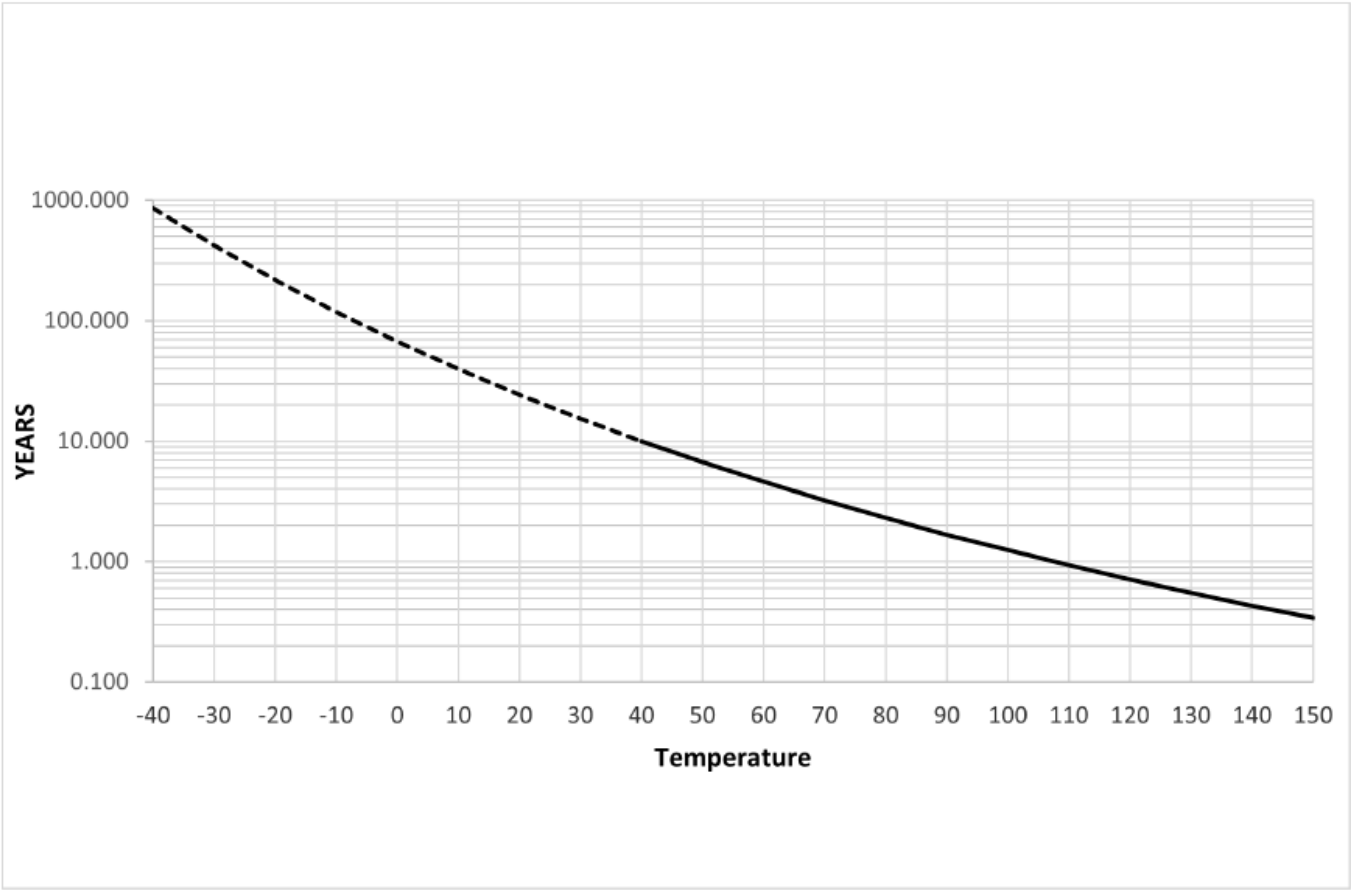
- Read-only data (Figure 4)
- Cycled data (Figure 5)

Page EEPROM data retention time vs temperature (Read-only data)



At average 40°C, the read-only data programmed in a page EEPROM product can be read for 100 years.

Page EEPROM data retention time vs temperature (cycled page)



At average 40°C, if the page is cycled, the data programmed in a page EEPROM product can be read for 10 years.

Data retention qualification method
Data retention qualification procedure for page EEPROM checks that the data remain readable with a safe programming level. The qualification method consists in storing the part in an oven at 150°C during 3000 hours with no DC voltage on pin VCC. Then the part content is checked. The data retention follows an Arrhenius law, this permits to extrapolate, from the different qualification tests performed at different temperatures, the page EEPROMs data retention performance. These limits are above the safe value defined in datasheets.

Application data retention strategy
To evaluate the data retention, it is recommended to evaluate the amount of time during which the end application remains within a same temperature range. A good data retention evaluation should:

- Define the time (in years) during which the Page EEPROM remain inside each temperature range (that is a typical temperature profile of the end application)
- Estimate the data retention value for each temperature range with the following equation:

$$\sum_{i=1}^{n} \frac{\text{Number of years at temp}(i)}{\text{Max number of years specified for temp}(i)} \leq 1$$

If the result of the equation is inferior or equal to 1, it means the application data retention time respects the maximum data retention capability of the page EEPROM products.

Example
An application is running for 14 years at 30°C and 6 years at 50°C. The application does not cycle pages

intensively and its lifetime is 20 years. The equation helps the user to determine if the maximum data capability is reached with the application temperature range.

Example of data retention capability calculation

Temperature (°C)	Application temperature (years)(1)	Data retention capability (years)	Data retention usage (%)(2)
30	14	232	6
50	6	56	10.7
			TOTAL: 16.7%

1. The maximum data retention is determined with the Figure 4
2. The data retention capability is calculated with the [1]

The data is safe for 20 years, with only 16.7% of data retention capability used. It means the data might be safe longer and it demonstrates the excellent data retention capability of the page EEPROMS product.

Conclusion

The budget of 500 k cycles per page is defined by the number of page write and erase operations executed over the page. Page program operations and ECC are irrelevant regarding the cycling budget of page EEPROM products. Moreover, this cycling budget is not depending on the temperature and voltage ranges, which makes page EEPROM very handy. To guarantee this cycling budget of 500 k cycles, page EEPROM products have follow a robust qualification process, respecting the JEDEC JESD47 guidelines. Thanks to this qualification method, page EEPROM can reach a total cumulated cycle of 1 billion. To optimize the cycling endurance of page EEPROMs, two strategies are available:

1. The pages counting, monitors the write endurance of each page with a dedicated counter byte.
2. The data class budget, distributes the cycling budget of a data over several locations and avoids max stress on a same area.

The second strategy is recommended when the application budget cycle is known. The first one, more flexible but less easy-to-use should be used if the application cycling budget is unknown. The retention capability of page EEPROM demonstrates the high quality of these products. This quality is possible thanks to a strong qualification process and the ECC (error code correction) which guarantees 100 years of retention for pages not intensively cycled and 10 years for pages intensively cycled pages. This application note can help users to calculate their application data retention capability (see Section 3.4 Application data retention strategy) and ensures the data safety stored in the page EEPROM products.

Document revision history

Date	Version	Changes
16-Feb-2023	1	Initial release.

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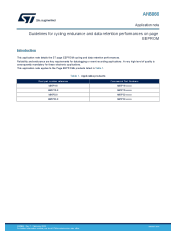
Documents / Resources

	**ST EEPROM Cycling and Data Retention Performances** [pdf] User Guide AN5866, EEPROM Cycling and Data Retention Performances, EEPROM, Cycling and Data Retention Performances

References

- **STMicroelectronics: Our technology starts with you**
- **STMicroelectronics Trademark List - STMicroelectronics**